

**AMENDMENTS TO THE CLAIMS**

The listing of claims below replaces all prior versions of claims in the application.

1. (Currently amended): A semiconductor device comprising a plurality of alignment marks formed over a semiconductor wafer,  
each of the alignment marks comprising a micronized pattern,  
the micronized pattern having a size smaller than a resolution limit of an alignment sensor of field image alignment detecting positions of the alignment marks, [[and]]  
the micronized pattern having a pattern forming margin larger than a pattern forming margin which a device pattern formed over the semiconductor wafer has, and wherein all of the alignment marks formed in the entire alignment mark area have the same shape so as to generate about the same field image alignment signal.

2. (Original): A semiconductor device according to claim 1, wherein  
the micronized pattern is a line-and-space pattern.

3. (Original): A semiconductor device according to claim 2, wherein  
each of lines constituting the line-and-space pattern are divided into a broken line having a plurality of segments.

4. (Original): A semiconductor device according to claim 3, wherein  
positions of the divisions between the plurality of segments of the lines are offset from those of the divisions between the plurality of segments of their adjacent lines.

5-12. (Cancelled)

13. (Currently amended): A semiconductor device comprising a plurality of alignment marks formed over a semiconductor wafer,

each of the alignment marks being divided by a micronized line-and-space pattern into a plurality of lines extending along a first direction, [[and]]

each of the plural lines being divided into a broken line having a plurality of segments which are arranged in the first direction only, and wherein all of the alignment marks formed in the entire alignment mark area have the same shape so as to generate about the same field image alignment signal.

14. (Original): A semiconductor device according to claim 13, wherein positions of the divisions between the plurality of segments of the lines are offset from those of the divisions between the plurality of segments of their adjacent lines.

15. (Previously presented): A semiconductor device according to claim 13, wherein a margin in which the micronized pattern is formed is larger than a margin for a device pattern to be formed on the semiconductor wafer.

16. (Previously presented): A semiconductor device according to claim 14, wherein a margin in which the micronized pattern is formed is larger than a margin for a device pattern to be formed on the semiconductor wafer.